NTMS5835NL

Power MOSFET

40 V, 12 A, 10 mΩ

Features

- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	9.2	A
		T_A = 70°C		7.4	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	1.5	W
		T_A = 70°C		1.0	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	t ≤10 s	T_A = 25°C	I_D	12	A
		T_A = 70°C		9.6	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.6	W
		T_A = 70°C		1.6	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	48	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	20	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 40 V, V_{GS} = 10 V, L = 0.1 mH)			EAS	69	mJ
			IAS	37	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

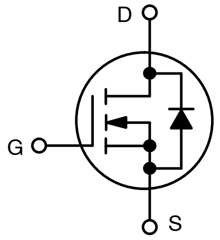
Parameter	Symbol	Value	Unit
Junction−to−Ambient Steady State (Note 1)	$R_{\theta JA}$	82	°C/W
Junction−to−Ambient – t ≤10 s (Note 1)	$R_{\theta JA}$	49	
Junction−to−Foot (Drain) (Note 1)	$R_{\theta JF}$	21	
Junction−to−Ambient Steady State (Note 2)	$R_{\theta JA}$	121	

1. Surface−mounted on FR4 board using 1 sq−in pad (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface−mounted on FR4 board using 0.155 in sq ($100 mm^2$) pad size.

ON Semiconductor®

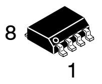
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	10 mΩ @ 10 V	12 A
	14 mΩ @ 4.5 V	

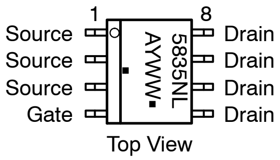


N−CHANNEL MOSFET

MARKING DIAGRAM/ PIN ASSIGNMENT



SO−8
CASE 751
STYLE 12



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS5835NLR2G	SO−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

April, 2011 − Rev. 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				16		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			1	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0	1.85	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				7.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A			8.2	10	mΩ
		V_{GS} = 4.5 V, I_D = 10 A			10.3	14	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 10 A			10		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			2115		pF
Output Capacitance	C_{OSS}				315		
Reverse Transfer Capacitance	C_{RSS}				220		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 10 A			40	50	nC
		V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 10 A			20	23	
Threshold Gate Charge	$Q_{G(TH)}$				2.0		
Gate−to−Source Charge	Q_{GS}				7.0		
Gate−to−Drain Charge	Q_{GD}				9.5		
Plateau Voltage	V_{GP}				3.3		V
Gate Resistance	R_G				1.2		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 10 A, R_G = 2.5 Ω			15		ns
Rise Time	t_r				45		
Turn−Off Delay Time	$t_{d(OFF)}$				22		
Fall Time	t_f				9.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.785		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 10 A			26		ns
Charge Time	t_a				13		
Discharge Time	t_b				13		
Reverse Recovery Charge	Q_{RR}				17		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

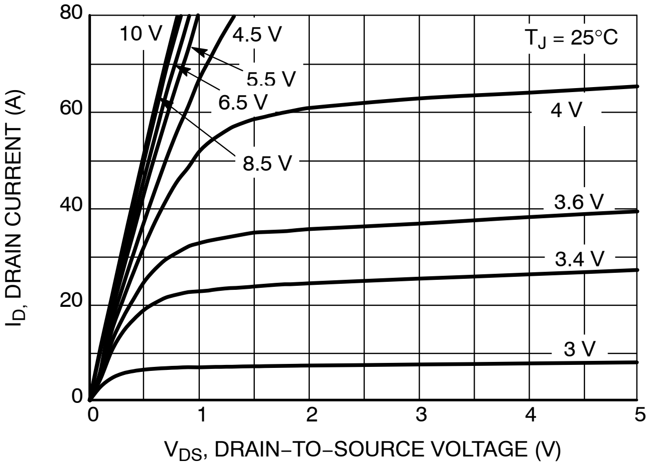


Figure 1. On−Region Characteristics

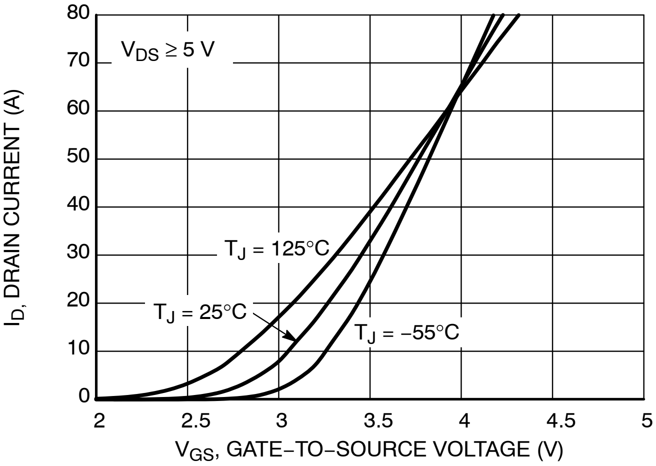


Figure 2. Transfer Characteristics

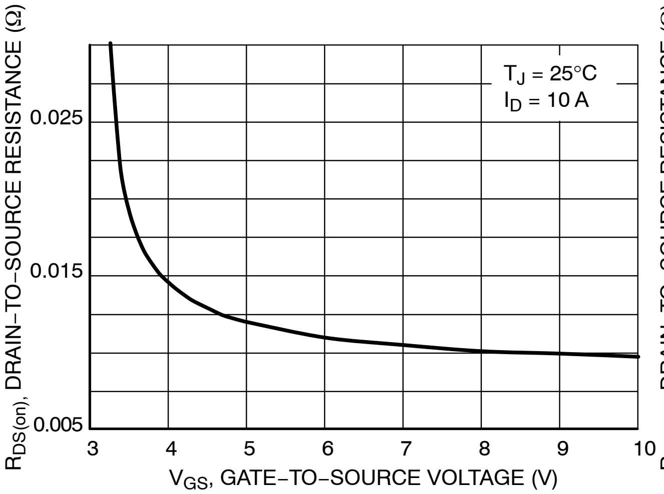


Figure 3. On−Resistance vs. Gate−to−Source Voltage

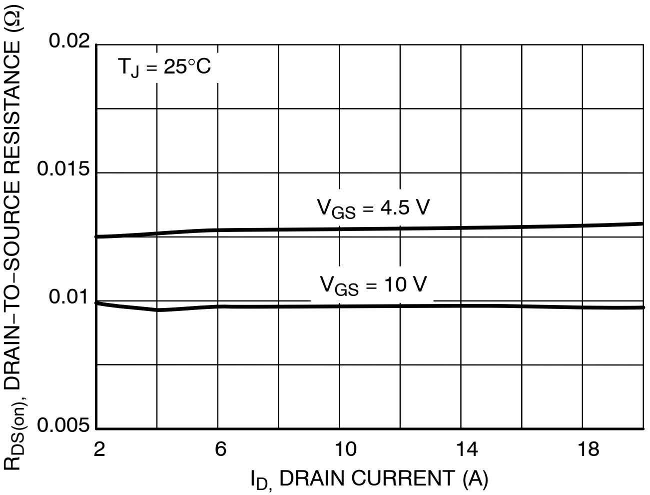


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

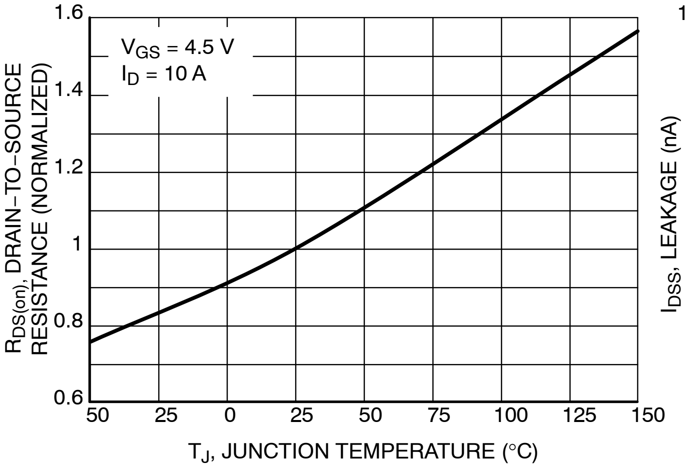


Figure 5. On−Resistance Variation with Temperature

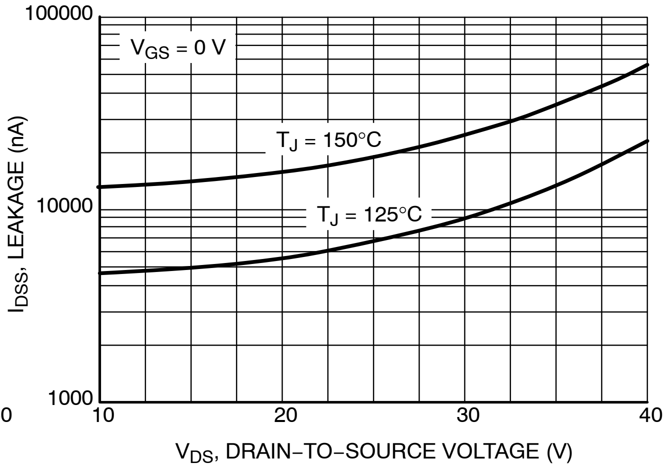


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

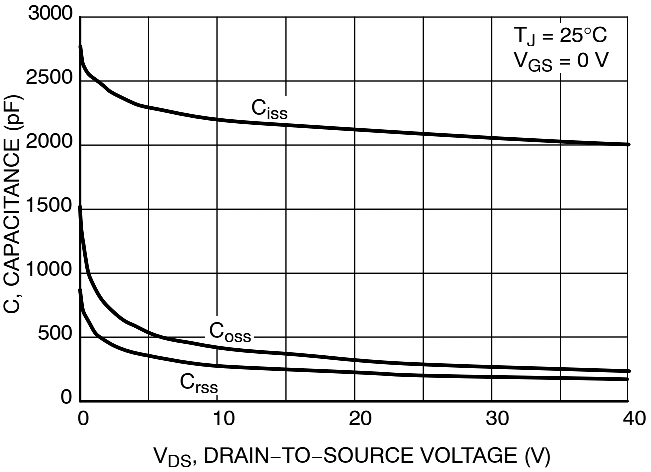


Figure 7. Capacitance Variation

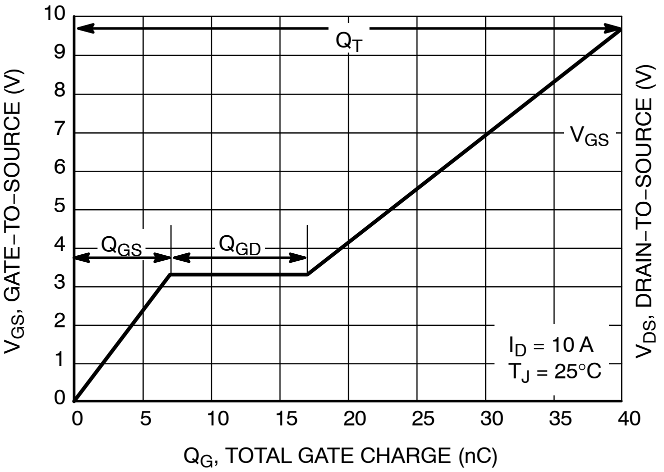


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

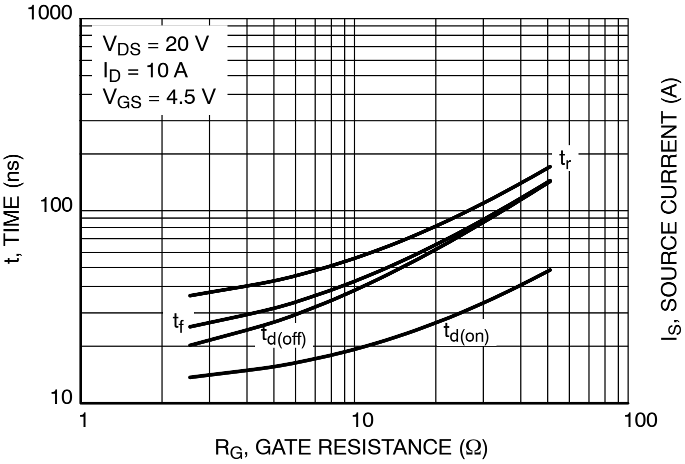


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

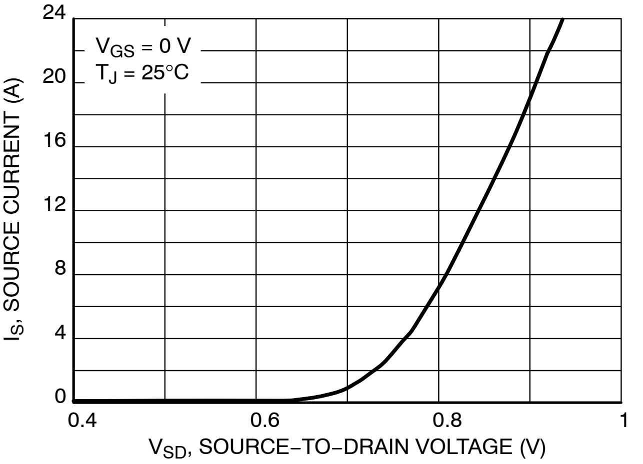


Figure 10. Diode Forward Voltage vs. Current

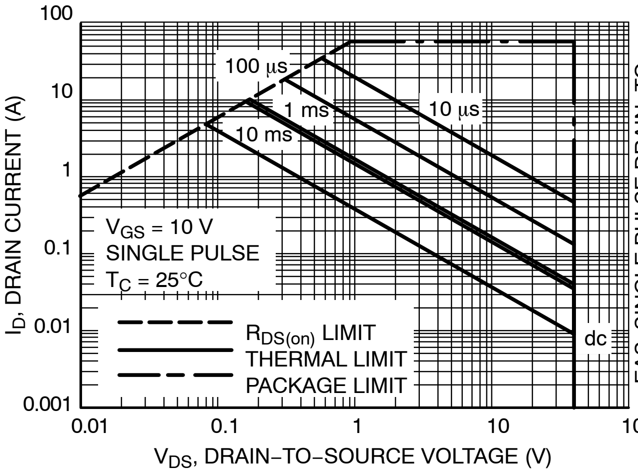


Figure 11. Maximum Rated Forward Biased Safe Operating Area

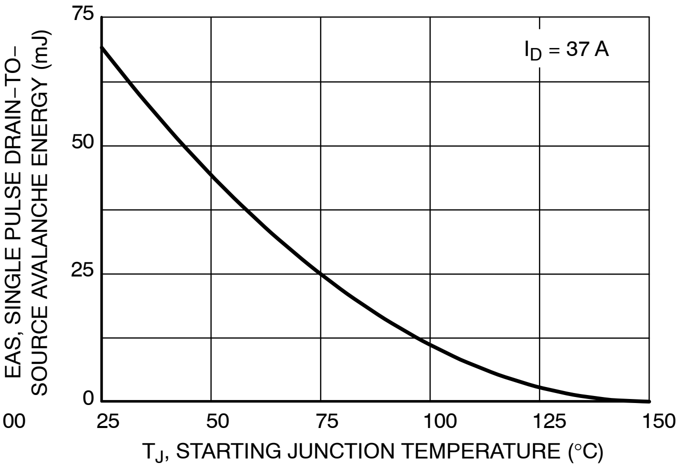


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

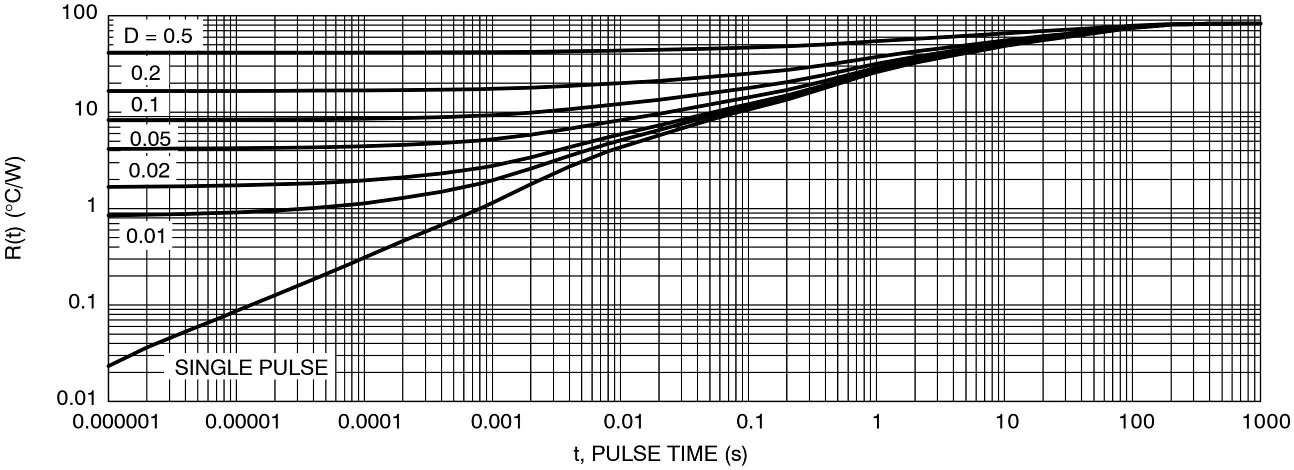
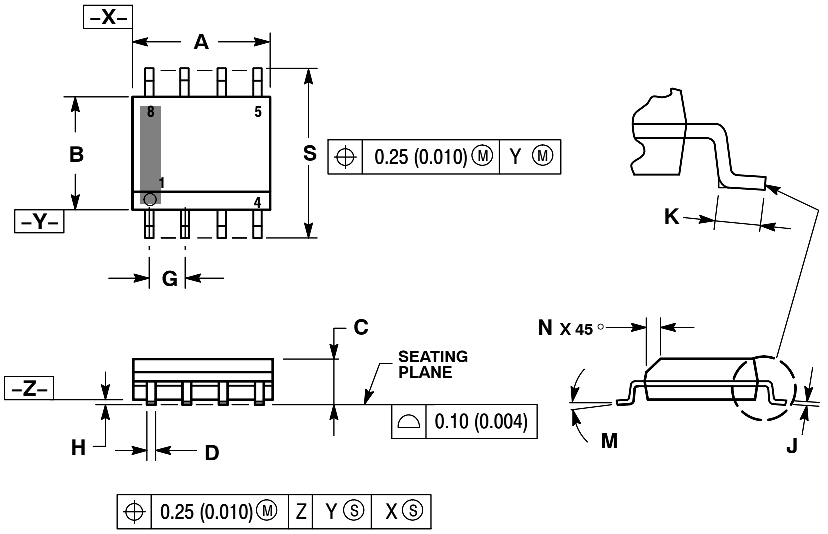


Figure 13. Thermal Response

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AK

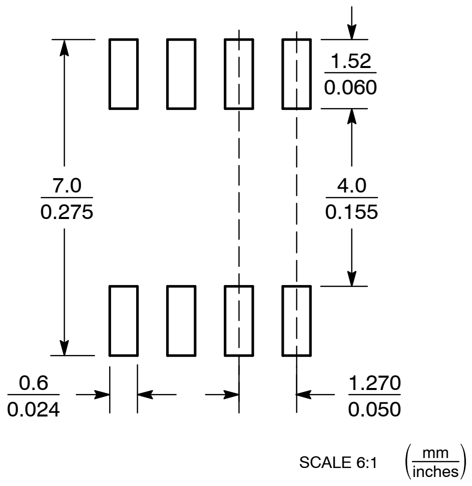


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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